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A MULTI-STAGE DELAY CLOCK GENERATOR

Abstract

The present invention provides a multi-stage delay clock generator including: a plurality of delay cells, each delay cell generating a delay signal to a subsequent delay cell in response to a delayed clock signal from a preceding delay cell and a delay control signal where a first delay cell among the plurality of delay cells receives an external clock signal, and each subsequent delay cell comprises a smaller delay step than the current delay cell; a phase detector, responsive to the external clock signal and a feedback clock signal, for generating a lock control signal; an integrator, responsive to the lock control signal, for generating the delay control signal; and a control unit for programming the delay cells.